Claims:

1. Reconfigurable signal processing architecture including a reconfigurable data processing module in which data is input to the module in a packet frame structure including configuration frames and processing frames, each frame including a header having at least one mode selection bit indicating whether the frame contains reconfiguration data or processing data, and in which the module is operable in a reconfiguration mode or a processing mode according to the content of the frame header and mode selection bits are separated from data in each frame and used to control mode selection logic in the module determining how incoming data is handled.

2. Architecture as claimed in claim 1 including a plurality of reconfigurable data processing modules each of which receives data in said packet frame structure and each of which is operable in a reconfiguration mode or a processing mode according to the content of the frame header.

3. Architecture as claimed in claim 2 in which the frame header contains at least one mode selection bit for each of the modules.

4. Architecture as claimed in claim 3 in which the mode selection bits are decoded by a single decoder serving a plurality of modules.

5. Architecture as claimed in claim 4 in which the decoded mode selection data is supplied to the modules in parallel.

6. Architecture as claimed in any of claims 2 to 5 in which the modules are connected to each other in series.

7. Architecture as claimed in any preceding claim in which the or each module is additionally operable in a bypass mode in which incoming data is not acted on by the module and in which the header additionally indicates whether or not the module is to act on the data.

8. A radio transmitter and/or receiver in which signals are processed digitally after reception/before transmission, in which at least some components of the digital processing section of the transmitter/receiver are configurable and incorporate architecture as claimed in any preceding claim.

9. Architecture as claimed in any preceding claim in which default/start up configuration data is supplied to the module(s) from memory outside the module(s).